WHAT IS CLAIMED IS:

1. A method of generating an output control signal in response to a read command for a synchronous semiconductor memory device, the method comprising the steps of:

generating a first clock signal from an external clock signal;

generating a second clock signal from the external clock signal;

passing the first clock signal through a delay circuit to provide a compensated first clock signal; and

generating the output control signal based on a Column Address Strobe ("CAS") latency signal, the compensated first clock signal and the second clock signal.

2. The method according to Claim 1, wherein the compensated first clock signal and the second clock signal are synchronized to the same cycle of the external clock signal.

3. The method according to Claim 1, wherein the first clock signal is generated from an input delay locked-loop circuit so that the first clock signal is synchronized with the external clock signal after the lapse of an input locking time and wherein the second clock signal is generated from an output delay locked-loop circuit so that the second clock signal is synchronized with the external clock signal after the lapse of an output locking time; wherein the input locking time is different from the output locking time.

4. The method according to Claim 1, wherein the step of passing the first clock signal through a delay circuit to provide a compensated first clock signal comprises passing the first clock signal through a delay circuit that delays the first clock signal by an integer number of clock cycles.

5. The method according to Claim 1, wherein the step of passing the first clock signal through a delay circuit to provide a compensated first clock signal comprises passing the first clock signal through one or more unit cycle delay circuits.

6. The method according to Claim 5, wherein the number of unit cycle delay circuits that the first clock signal is passed through is determined by which one of a plurality of fuses is left uncut.

7. The method according to Claim 6, wherein the number of unit cycle delay circuits that the first clock signal is passed through is further based on the value of the Column Address Strobe ("CAS") latency signal.

8. A method of operating a synchronous semiconductor memory device, the method comprising the steps of:

generating a first clock signal and a second clock signal that are synchronized to different cycles of an external clock signal;

synchronizing the first clock signal and the second clock signal to the same cycle of the external clock signal; and

generating a data output control signal in response to a read information signal, a Column Address Strobe ("CAS") latency signal and the synchronized first and second clock signals.

9. The method according to Claim 8, wherein the first clock signal is an internal clock signal and the second clock signal is an output control clock signal.

10. The method according to Claim 8, wherein the step of synchronizing the first clock signal and the second clock signal to the same cycle of the external clock comprises delaying at least one of the first clock signal and the second clock signal by an integer number of clock cycles.

11. The method according to Claim 10, wherein the amount that the at least one of the first clock signal and the second clock signal are delayed varies based on the CAS latency signal.

12. The method according to Claim 10, wherein the step of delaying at least one of the first clock signal and the second clock signal by an integer number of clock cycles comprises passing the at least one of the first clock signal and the second clock signal through at least one unit cycle delay circuit.

13. A synchronous semiconductor memory device for storing data comprising:

a first clock signal generation circuit that generates a first clock signal that is synchronized with a first cycle of an external source clock;

a second clock signal generation circuit that generates a second clock signal that is synchronized with a second cycle of the external source clock;

an output control signal generating circuit that generates an output control signal in response to a read signal, a Column Address Strobe ("CAS") latency signal, the first clock signal and the second clock signal;

a first transfer/delay circuit coupled between the first clock signal generation circuit and the output control signal generating circuit that delays the first clock signal before it is passed to the output control signal generating circuit so that the first clock signal and the second clock signal are synchronized to the same cycle of the external source clock; and

an output buffer that outputs the data in response to the output control signal.

14. The synchronous semiconductor memory device according to Claim 13, wherein the first transfer/delay circuit comprises a plurality of transfer/delay units that act to delay the first clock signal by zero, one, two or three clock cycles.

15. The synchronous semiconductor memory device according to Claim 13, further comprising a second transfer/delay circuit coupled between the second clock signal generation circuit and the output control signal generating circuit that delays the second clock signal before it is passed to the output control signal generating circuit so that the second clock signal and the first clock signal are synchronized to the same cycle of the external source clock.

16. The synchronous semiconductor memory device according to Claim 15, wherein the second transfer/delay circuit comprises a plurality of transfer/delay units that act to delay the second clock signal by zero, one, two or three clock cycles.

17. The synchronous semiconductor memory device according to Claim 13, wherein the first transfer/delay circuit varies the delay time between the first

clock signal and the delayed version of the first clock signal based on the CAS latency signal.

18. The synchronous semiconductor memory device according to Claim 13, wherein the first clock signal is an internal clock signal and the second clock signal is an output control clock signal.

19. The synchronous semiconductor memory device according to Claim 13, wherein the first transfer/delay circuit comprises:

a plurality of delay circuits, each of which includes a plurality of unit cycle delay circuits that act to delay the first clock signal by zero, one, two or three cycles; and

a first multiplexer that, based on the CAS latency signal, selects the output of one of the delay circuits.

20. The synchronous semiconductor memory device according to Claim 19, wherein each of the plurality of delay circuits comprises:

a first unit cycle delay circuit which delays the internal clock signal by one cycle of the internal clock signal;

a second unit cycle delay circuit which delays the internal clock signal that was delayed via the first unit cycle delay circuit by one cycle of the internal clock signal;

a third unit cycle delay circuit which delays the internal clock signal that was delayed via the second unit cycle delay circuit by one cycle of the internal clock signal;

a first fuse which transfers the internal clock signal to the first multiplexer without delay when the first fuse is not cut;

a second fuse which transfers the internal clock signal that was delayed via the first unit cycle delay circuit to the first multiplexer when the second fuse is not cut;

a third fuse which transfers the internal clock signal that was delayed via the second unit cycle delay circuit to the first multiplexer when the third fuse is not cut; and

a fourth fuse which transfers the internal clock signal that was delayed via the third unit cycle delay circuit to the first multiplexer when the fourth fuse is not cut.

21. A synchronous semiconductor memory device comprising:

a first clock signal generation circuit that generates a first clock signal that is synchronized with a first cycle of an external source clock;

a second clock signal generation circuit that generates a second clock signal that is synchronized with a second cycle of the external source clock;

a delay circuit that operates on at least one of the first clock signal and the second clock signal to synchronize the first clock signal and the second clock signal to the same cycle of the external source clock; and

an output control signal generation circuit that generates an output control signal in response to a read information signal, a Column Address Strobe ("CAS") latency signal and the synchronized first and second clock signals.

22. The synchronous semiconductor memory device according to Claim 21, wherein the delay circuit comprises a plurality of transfer/delay units that act to delay the at least one of the first clock signal and the second clock signal by an integer number of clock cycles.

23. The synchronous semiconductor memory device according to Claim 22, wherein the amount that the at least one of the first clock signal and the second clock signal are delayed varies based on the CAS latency signal.